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Video encoder

Abstract:

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(54) Video encoder

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which uses a center-biased orthogonal searching procedure to match the block with a previously processed image. A zero block detector module (54) determines whether the block will generate a zero-valued block after being processed by a transform module 18 and a quantization module 20. If a zero-valued block is predicted, the transformation module 18 and the quantization module 20 are bypassed.

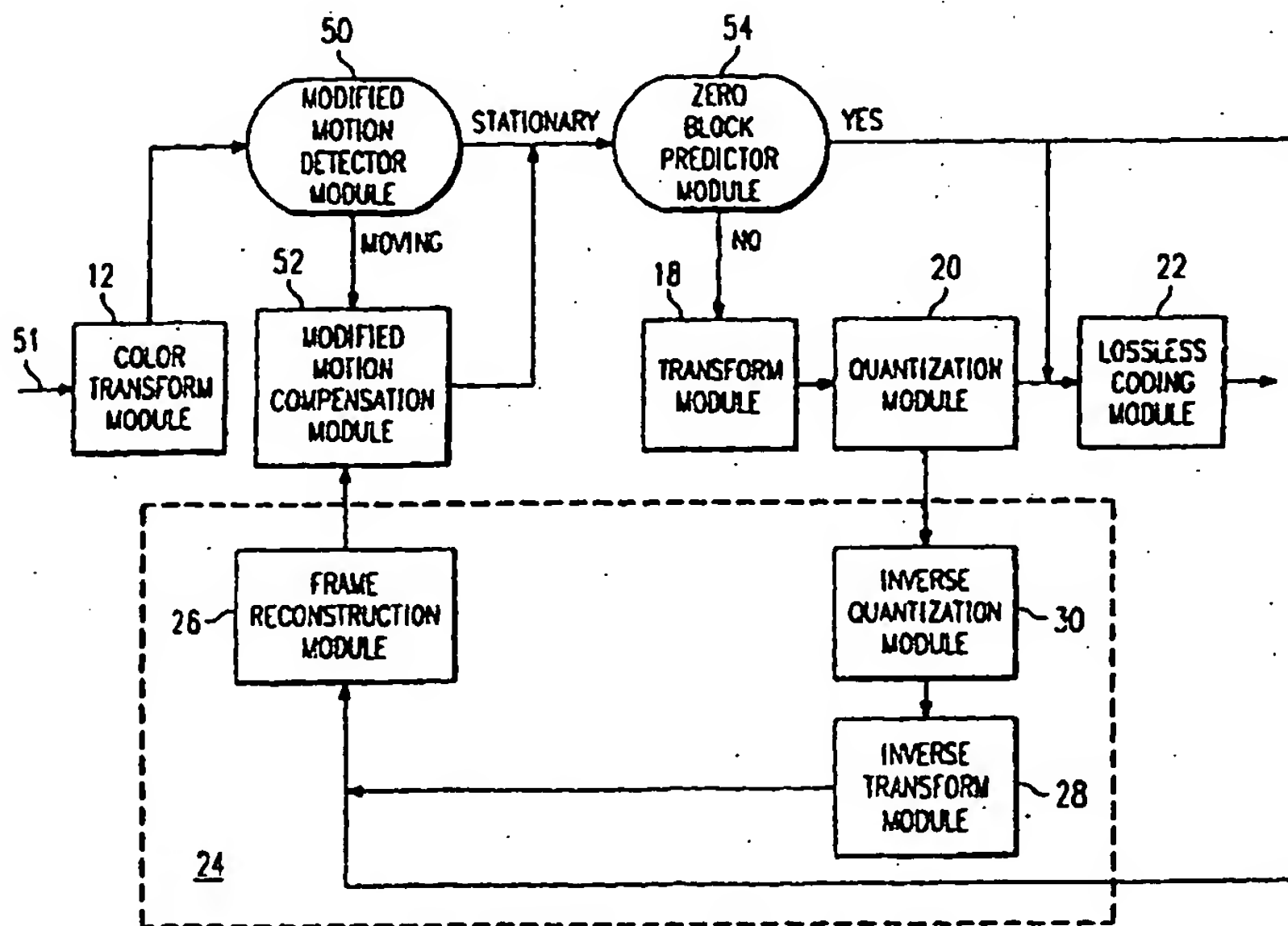


FIG. 3

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Description

TECHNICAL FIELD OF THE INVENTION

This invention relates to image processing and in particular to a method and system for improved encoding of video data.

BACKGROUND OF THE INVENTION

Image compression and decompression are used in a wide range of applications including video conferencing systems, video phones, and motion picture transmission. The conventional approach in these applications has been to use dedicated hardware for video coding, (i.e., image compression and decompression). The use of dedicated hardware, typically digital signal processors (DSPs), is required because the video coding process is computationally expensive and slow on general-purpose hardware. As a result, widespread use of these applications has been stymied by the costs associated with deploying the specialized hardware required to achieve good performance. It has been predicted, however, that these applications, in particular video conferencing, will become desktop commodities in the next few years. Improvements to the video coder and the video coding process are necessary to make this prediction a reality.

A diagram illustrating a video coding process in accordance with International Telecommunication Union (ITU) standard H.263, hereinafter referred to as the ITU H.263 standard, for video coding and encoding at very low bit-rates, such as at 28K bits per second, is shown in Fig. 1.

The video encoder shown in Fig. 1 includes a color transform module 12, a motion detector module 14, a motion compensation module 16, a transform module 18, a quantization module 20, and a coding module 22. Also included is a feedback module 24 which includes an inverse quantization module 30, an inverse transformation module 28, and a frame reconstruction module 26.

A video decoder, as shown in Fig. 2, performs the reverse process of the video coder and includes a bit-stream decoding module 40, the inverse quantization module 30, the inverse transform module 28, an inverse motion compensation module 42, and the frame reconstruction module 26.

In the video coding process, motion compensation performed by the motion compensation module 16 is the most time consuming phase. The transformation and quantization phases, performed by the transformation module 18 and the quantization module 20, respectively, are also expensive phases to perform.

However, with processor speeds doubling every two years, it is possible for software-only solutions to attain good performance and quality and to lower the costs associated with applications which require video

processing enough make image processing a commodity item in desktop computing environments.

To overcome the computational requirements of the various stages, the video processing applications in prior art systems employ dedicated DSPs to make the various computationally expensive stages execute faster. Use of dedicated hardware is a weakness of current video conferencing systems. Designing new hardware as the video coding standards change and evolve is expensive, time-consuming and substantially increases the cost of delivered systems. Not only do the high costs associated with dedicated hardware present a barrier against image processing applications becoming a desktop commodity solutions, but they also go against the latest trend in hardware/software solution to use open systems.

Thus, what is needed is a method and system to overcome the limitations and weaknesses of current video processing application implementations. In particular, what is needed is a method and system for video encoding which is computationally more efficient than those of the prior art and which are amenable to implementation using low-cost general-purpose DSPs or software-only solutions.

SUMMARY OF THE INVENTION

The present invention includes a video coding process which can be implemented on low-cost, general purpose DSPs or as a software only solution on a general purpose microprocessor to get acceptable performance. The present invention modifies the overall video coding process and augments it with optimizations which reduce the overall video coding computation time thereby making it viable to use the low-cost DSP solutions or a software-only solution, both of which permit acceptable performance on today's desktop CPUs.

One aspect of the present invention includes optimizations of the motion detection stage.

Another aspect of the present invention includes optimizations of the motion compensation stage.

Yet another aspect of the present invention includes the addition of a zero block prediction stage.

DESCRIPTION OF THE DRAWINGS

These and other features of the invention that will be apparent to those skilled in the art from the following detailed description of the invention, taken together with the accompanying drawings in which:

Fig. 1 is a block diagram depicting a prior art video encoder;

Fig. 2 shows a block diagram illustrating a prior art video decoder;

Fig. 3 illustrates a first embodiment of a video en-

coder in accordance with the present invention;

Fig. 4 depicts a second embodiment of a video encoder in accordance with the present invention;

Fig. 5 shows a third embodiment of a video encoder in accordance with the present invention;

Fig. 6 is a flow diagram illustrating the operation of a video encoder in accordance with the present invention;

Fig. 7 shows a flow diagram illustrating the operation of a modified motion detector module in accordance with the present invention;

Fig. 8 illustrates a flow diagram showing the operation of a modified motion compensation module in accordance with the present invention; and

Fig. 9 is a block diagram depicting the operation of a zero block predictor module in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

A video coder in accordance with the present invention, as shown in Fig. 3, includes several improvements to the video coder and video coding process of the prior art, shown in Fig. 1. The improvements shown in the video coder in accordance with the present invention as depicted in Fig. 3 provide for increased performance over video coders and video coding processes of the prior art. It is contemplated that the video coder and video coding process in accordance with the present invention are useful in any application using video coding techniques.

The present invention is implemented in C++ using Microsoft's Visual C++ compiler on a workstation which included in a Pentium processor. It is contemplated, however, that use of other languages and hardware configurations would be apparent to those skilled in the art.

The overall structure of the video coder in accordance with the present invention is shown in Fig. 3. As discussed hereinabove, the motion compensation stage and the transformation stage are among the most time consuming stages in a typical video coding process. The present invention provides for improvements to the motion detection stage as performed by modified motion detector module 50. The modified motion detector module 50 in accordance with the present invention determines whether to bypass the motion compensation stage performed by the modified motion compensation module 52. The modified motion compensation module 52 also includes improvements to the motion compensation stage over that of the motion compensation module 16 of the prior art.

The video coding process in accordance with the

present invention also includes the addition of a zero block prediction stage, performed by zero block predictor module 54. The zero block predictor module 54 determines whether or not to bypass the transformation and quantization stages. Each of these features are discussed in detail hereinbelow.

It is contemplated that other embodiments, in addition to that shown in Fig. 3, of the present invention are possible which also provide improvements to the video coder of the prior art. Another embodiment of the video coder in accordance with the present invention is shown in Fig. 4, which includes the modified motion compensation module 52. Fig. 5 illustrates yet another embodiment of video coder in accordance with the present invention which includes the modified motion detector module 50 and the zero block predictor module 54.

The operation of the video encoder shown in Fig. 3 is illustrated in Fig. 6. At block 60, the color transformation module 12 generates data signals from the video image signals input at 51.

The data signals are then input to the modified motion detector module 50 as shown at block 62 which determines whether movement is detected in the represented image. If, at decision block 64, movement is detected, the modified motion compensation module 52, as shown at block 66, compensates for that movement and operation continues at block 68. If, at decision block 64, movement is not detected, the motion compensation stage performed by the modified motion compensation module 52 is bypassed and operation continues at block 68.

At block 68, the zero block predictor module 54 determines whether the currently processing macroblock of data signals will generate a zero-valued macroblock after the transformation and quantization stages performed by the transform module 18 and the quantization module 20, respectively. If, at decision block 70, a zero-valued macroblock is predicted, the transformation and quantization stages are bypassed and operation continues at block 78.

If, at decision block 70, a zero-valued macroblock is not predicted, operation continues at block 72 where the data signals are transformed by the transform module 18. In the present invention, the transform module 18 performs a discrete cosine transformation but, it is contemplated that other transformations may be used. The transformed data signals are then quantized at block 74 by the quantization module 20. At block 76, the data signals of the currently processed image are used to generate an interpolated image which is fed back into the modified motion compensation module 52 at block 66.

The quantized data signals generated at block 74 are encoded at block 78 for further processing by the application which incorporates or uses the video coder of the present invention.

In the motion detection stage performed by the modified motion detector module 50, the operation of

which is illustrated in detail in Fig. 7, the macroblocks of the currently processing image processed are classified as either moving or stationary. In order to classify the macroblocks, the modified motion detection module 50 determines if the macroblock has moved based upon predetermined motion criteria. The modified motion detector module 50 then, using the predetermined motion criteria, compares the currently processing macroblock with a macroblock which is in the same location in the previous image, the interpolated image generated by the feedback module 24, as the currently processing macroblock is in the current image.

The pixel-by-pixel absolute difference between the macroblock in the currently processing image and the macroblock at the same location in the previous image is calculated. If the difference between a pixel in the currently processing image and a pixel in the same location in the previous image is above a predetermined threshold, then that pixel is classified as moving within that macroblock. If the number of pixels classified as moving are above a second predetermined threshold, then the macroblock is classified as moving, otherwise the macroblock is classified as stationary. If the macroblock is stationary then the motion compensation phase is skipped entirely and computation proceeds as shown in Fig. 6.

Returning to Fig. 7, if, at decision block 110, the modified motion detector module 50 is processing a macroblock in the first frame of data representing the current image (i.e., if it is an INTRA coded block), that macroblock is classified as stationary at block 134 and processing by the modified motion detector module 50 terminates. If, at decision block 110, the current macroblock is not the first macroblock being processed, processing continues at block 112 where a counter and a maximum data signal indicator are initialized. Operation then continues at block 114 where the first pixel in the currently processing macroblock is retrieved.

If, at decision block 116, the signal value of the current pixel in the currently processing macroblock is greater than the current value of the maximum data signal indicator, then the value of the maximum data signal indicator is replaced with the signal value at block 118 and operation continues at block 120. If, at decision block 116, the signal value of the current pixel is not greater than the current value of the maximum data signal indicator then operation continues at block 120 where the modified motion detector module 50 determines the difference between the signal value of the current pixel and the signal value of the pixel in the same location in the previous image.

If, at decision block 122, that difference is greater than the first predetermined threshold, the counter is incremented at block 124 and operation continues at decision block 126. If, at decision block 122, the difference is not greater than the first predetermined threshold, operation also continues at decision block 126 where, if there are more pixels in the currently processing macro-

block, the next pixel is retrieved at block 128 and operation continues at decision block 116. If, at decision block 126, all pixels in the current macroblock have been processed, a determination is made at decision block 130 as to whether the counter is above the second predetermined threshold.

If, at decision block 130, the counter is above the second predetermined threshold, the macroblock is classified as moving at block 132. If, at decision block 130, the counter is not above the second predetermined threshold, the macroblock is classified as stationary at block 134. Operation in the modified motion detector module 50 then terminates.

Returning to Fig. 6, if, as shown at decision block 64, the modified motion detector module 50 classifies the current macroblock as moving, the motion compensation stage performed by the modified motion compensation module 52 is not bypassed. The modified motion compensation module 52 operates as shown in Fig. 8.

The motion compensation module 16 in video coders of the prior art and the modified motion compensation module 52 in accordance with the present invention both use a search procedure to find a best matching macroblock in the previous image then both perform a half-pel search around the best matching macroblock in an interpolated version of the represented image. If a full search block matching procedure is used, as in the motion compensation module 16 in video coders of the prior art, the motion compensation phase is an order of magnitude more expensive (in terms of adds and multiplies) than any other phase of the video coding process. Therefore, to reduce the complexity of the motion compensation stage, the modified motion compensation module 52 of the present invention includes several improvements.

As shown in block 80 in Fig. 8, the modified motion compensation module 80 first retrieves the macroblock from the previous image which is in the same location in the previous image as the currently processing macroblock is in the current image. The modified motion compensation module 52 then determines, at block 82, the sum of the absolute difference between the retrieved macroblock from the previous image and the currently processing macroblock in the current image.

If, at decision block 84, the sum of absolute difference between the macroblock in the currently processing image and the macroblock at the same location in the previous image is below a certain predetermined threshold, then no further search is done and processing continues at block 92 where the retrieved macroblock in the previous image is chosen as the best matching block.

If, at decision block 84, the sum is above the predetermined threshold, processing continues at block 86 where eight neighboring points around the center of the retrieved macroblock in the previous image are determined. The modified motion compensation module 52 then determines, at block 88, the sum of the absolute

difference between the pixels in the currently processing macroblock and each macroblock in the previous image centered around one of the eight neighboring points.

This center biased orthogonal search algorithm (C-OSA) for block matching used by the motion compensation module 52 of the present invention is an optimization of the orthogonal search algorithm (OSA) described in the article entitled "An Efficient Block-Matching Algorithm for Motion-Compensated Coding" by A. Puri, et al. and published in Proceeding IEEE ICASSP 1987 on pages 25.4.1-25.4.4. The C-OSA used in the modified motion compensation module 52 in the present invention performs a quick search on a set of eight neighboring points (+ or - one pixel in each direction and along the diagonals) centered around the search point in the retrieved macroblock in the previous image.

In the center-biased search procedure used in the modified motion compensation module 52 of the present invention, if, at decision block 90, the best-match occurs at the center, then no further search is done and processing continues at block 92 where the macroblock centered around that best matching point is chosen. If, however, at decision block 90, the best match occurs at one of the eight neighboring points, processing continues at decision block 94.

If, at decision block 94, the best match is at an orthogonal point (a point which is + or - p pixel, where p is equal to 7, in any direction from the center point, i.e., not one of the points along a diagonal) then the searching procedure performed by the modified motion compensation module 52 in the present invention proceeds as in the OSA procedure described in Puri, et al. If, however, at decision block 94, the best match occurs instead at one of the eight neighboring points, then a new set of eight neighboring points is selected with that best matching point as the center point. The best match amongst this new set of eight neighboring points is returned at block 100 as the result. Note that in the new set of eight neighboring points, not all eight points have to be recomputed since some were already computed previously.

It is worthwhile noting that the approach taken by the modified motion compensation module 52 favors motion compensation on images where there is relatively little motion between successive images, which is typical of video conferencing applications. The C-OSA procedure used by the modified motion compensation module 52 of the present invention includes a quick test to find the best matching block in a very small search area. In the worst case the modified motion compensation module 52 of the present invention does a full orthogonal search which is still less complex and produces good results. The complexity of the C-OSA used in the modified motion compensation module 52 of the present invention is $16+4\log_2 w$, where w is search distance in pixels, typically plus or minus 15 pixels.

Finally, as shown at block 102, the modified motion compensation module 52 of the present invention ap-

plies the OSA procedure described in Puri, et al. to the half-pel motion compensation search. The half-pel search is done on the interpolated image in a search area of plus or minus one pixel in all directions and along the diagonals. Surprisingly, this took more than a substantial proportion of the overall motion compensation time used by the modified motion compensation module 52 since the full-pel search described hereinabove is already quite efficient. Applying the OSA procedure described in Puri, et al. on the half-pel search substantially reduced the number of search points. Also, the search area for border blocks is much smaller, since part of the area is not within the picture boundary, which provided additional savings in computation time.

Results obtained from the C-OSA and OSA procedures applied to full-pel and half-pel search, respectively, by the modified motion compensation module 52 were very close to an exhaustive search with no noticeable degradation of image quality and resulted in an order of magnitude speed up of motion compensation when compared to the exhaustive search. On several ITU H.263 standard test images, including the "Miss America" image, motion compensation takes less than 12% of the total computing time with less than a .01 dB decrease in signal-to-noise ratio.

Returning to Fig. 6, on typical image sequences, e.g., on ITU test image sequences, less than 30% of INTER coded blocks had non-zero values after the quantization stage at 74 but all blocks had to go through the expensive transformation stage at block 72. Furthermore, the non-zero valued blocks had only one or two non-zero coefficients. To exploit the above observation a zero block prediction stage at 70 performed by the zero block predictor module 54 is included after the motion compensation stage at 66.

The modified motion detector module 50, as described in the hereinabove, classifies macroblocks as either moving or stationary. The modified motion detector module 50 also records the maximum signal value and the number of stationary pixels in the entire macroblock. Based on a quantization value which changes as processing progresses, this information is used by the zero block predictor module 50 to determine or predict whether a macroblock will have all zero values after the transformation and quantization stages. If a zero-valued block is predicted, then the transformation and quantization stages, at 72 and 74, respectively, are skipped and a zero value block is generated.

The operation of the zero block predictor module 54 is shown in Fig. 9. At block 140, the prediction is set to "no". If, at decision block 142, a macroblock within the first frame is being processed, processing in the zero block predictor module 54 terminates. Otherwise, at block 144, the zero block predictor module 54 applies heuristics using the maximum signal value, the number of stationary pixels, and the current quantization value to determine if the current macroblock will generate a zero-valued block after the transformation and quanti-

zation stages. If, at decision block 146, a zero-valued block is predicted, then the prediction is set to "yes" at block 148 and processing in the zero block predictor module 54 terminates.

The heuristics used by the zero block predictor module 54 are only applied to INTER coded blocks. On average this saves about 30% of the blocks from going through the transformation and quantization stages. However, because of the conservative nature of the heuristic used by the zero block predictor module 54, 40% of the blocks which would have been zero valued blocks still went through the expensive transformation and quantization stages. It is contemplated, however, that the percentage of the blocks that are predicted as zero-valued blocks by the zero block predictor module 54 can be increased as the heuristics used are improved.

Before this optimization was applied, the transformation and quantization stages consumed about 30% of the total processing time. This reduced to about 18% after the above optimizations were applied. It is contemplated that the processing time can be further reduced if improved heuristics for predicting zero-valued blocks are applied. The overall video coding process in the present invention achieves about a 5-6 fold increase over the video coding process the ITU H.263 standard. Thus, the video coding process in accordance with the present invention is computationally more efficient and amenable to implementation using low-cost DSPs or software-only solutions.

The techniques and concepts described in this invention were developed specifically for the video coding process used by video conferencing systems. However, it is contemplated that the present invention is also applicable to any application which uses video coding techniques for image compression.

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention.

Claims

1. A video encoder comprising:

a color transform module for receiving input video signals and for generating a first set of data signals representing a current image, including a plurality of pixels;
a motion detector module coupled to said color transform module and responsive to said first set of data signals for generating a classification signal classifying said current image as moving or stationary;
a motion compensation module responsive to said classification signal generated by said mo-

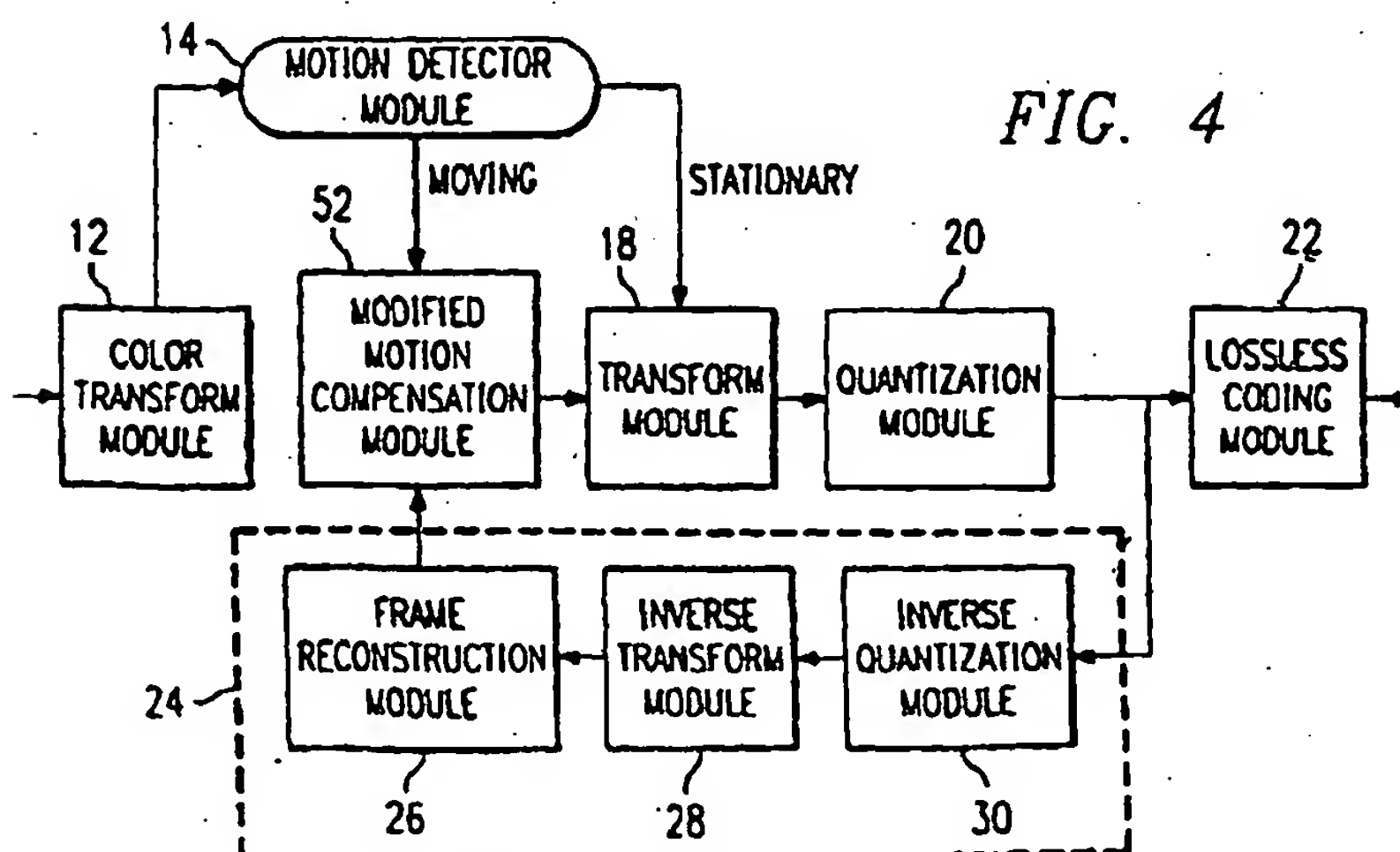
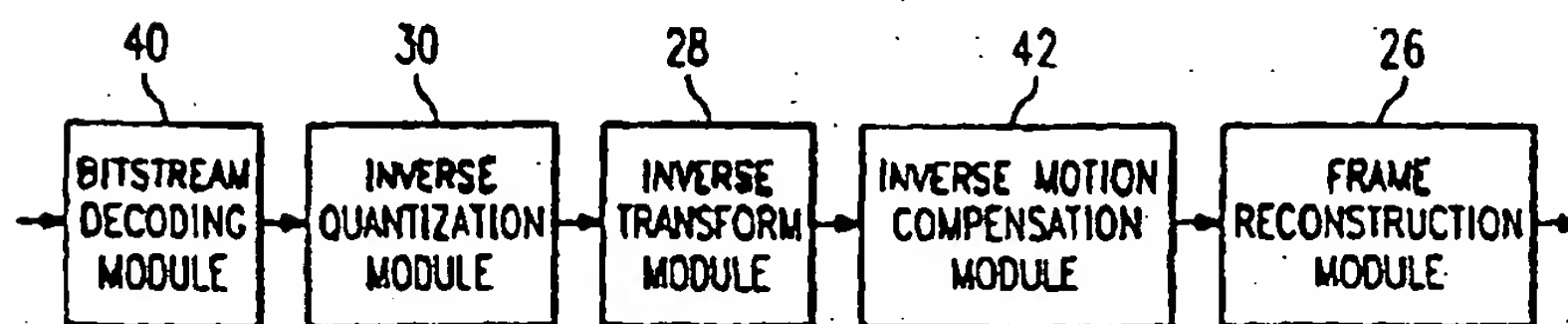
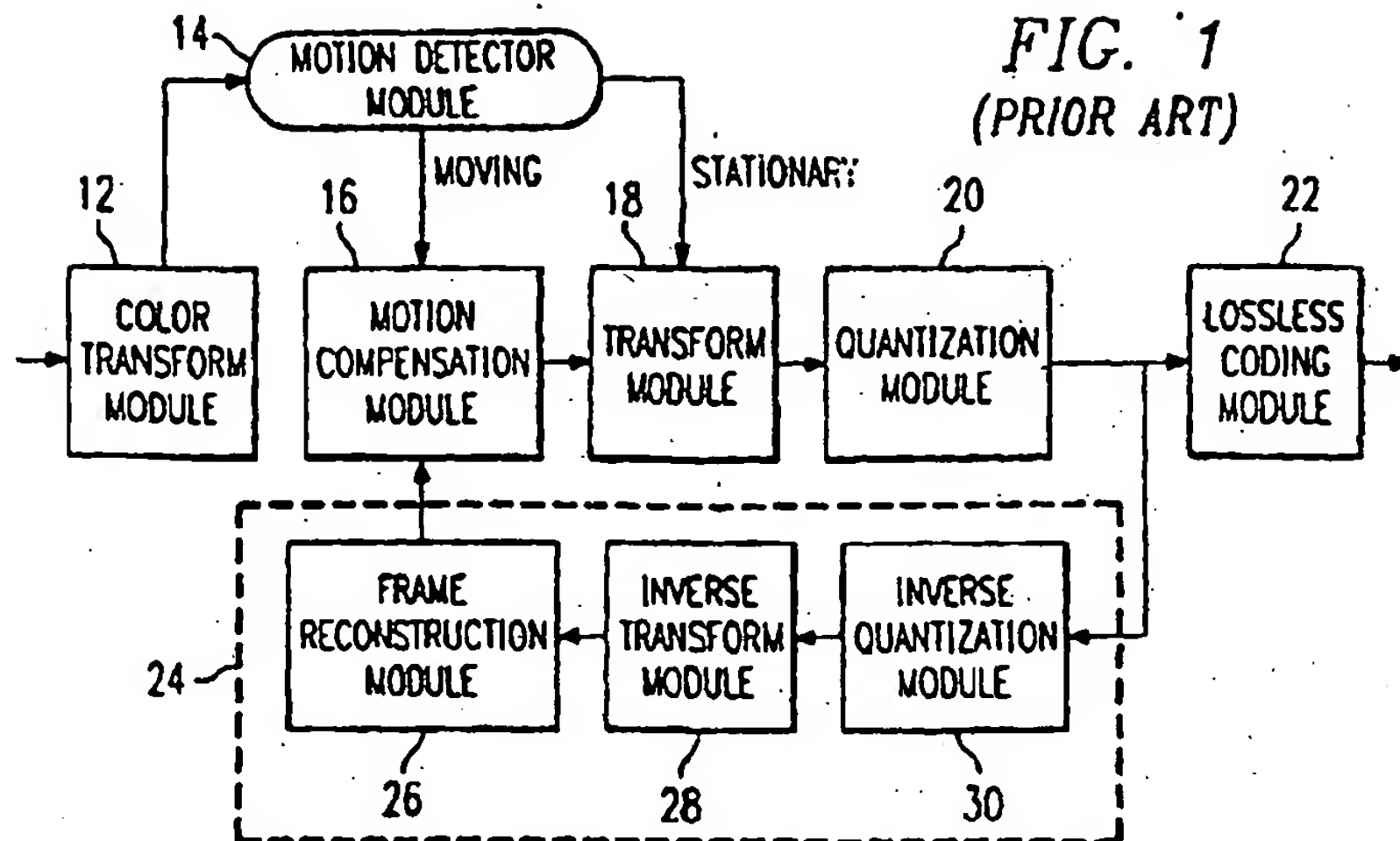
tion detector module and a second set of data signals representing a previous image generated by a feedback module for compensating for motion in said current image;

a computational module responsive to said modified motion compensation module for generating digitized data signals from said first set of data signals;

said feedback module responsive to said digitized data signals for generating said second set of data signals for input to said motion compensation module; and

a coding module responsive to said digitized data signals for generating encoded data signals.

2. The video encoder as claimed in Claim 1, wherein said motion compensation module is capable of applying a center-biased orthogonal search technique.
3. The video encoder as claimed in Claim 1 or Claim 2, wherein said motion detector module is further responsive to a maximum value signal and a counter signal indicative of how many of said pixels are classified as stationary.
4. The video encoder as claimed in Claim 3, further comprising: a zero block predictor module responsive to first set of data signals, said maximum value signal and said counter signal for generating a zero block signal indicative of whether computation on said first set of data signals will generate non-zero data; and
said computational module responsive to said zero block signal for generating said digitized data signals from said first set of data signals.
5. The system of any Claims 2 to 4, wherein said motion compensation module is operable to perform a full pel search in accordance with said center-biased orthogonal search technique.
6. The system of any of Claims 2 to 4, wherein said motion compensation module is operable to perform a half pel search in accordance with an orthogonal search technique.



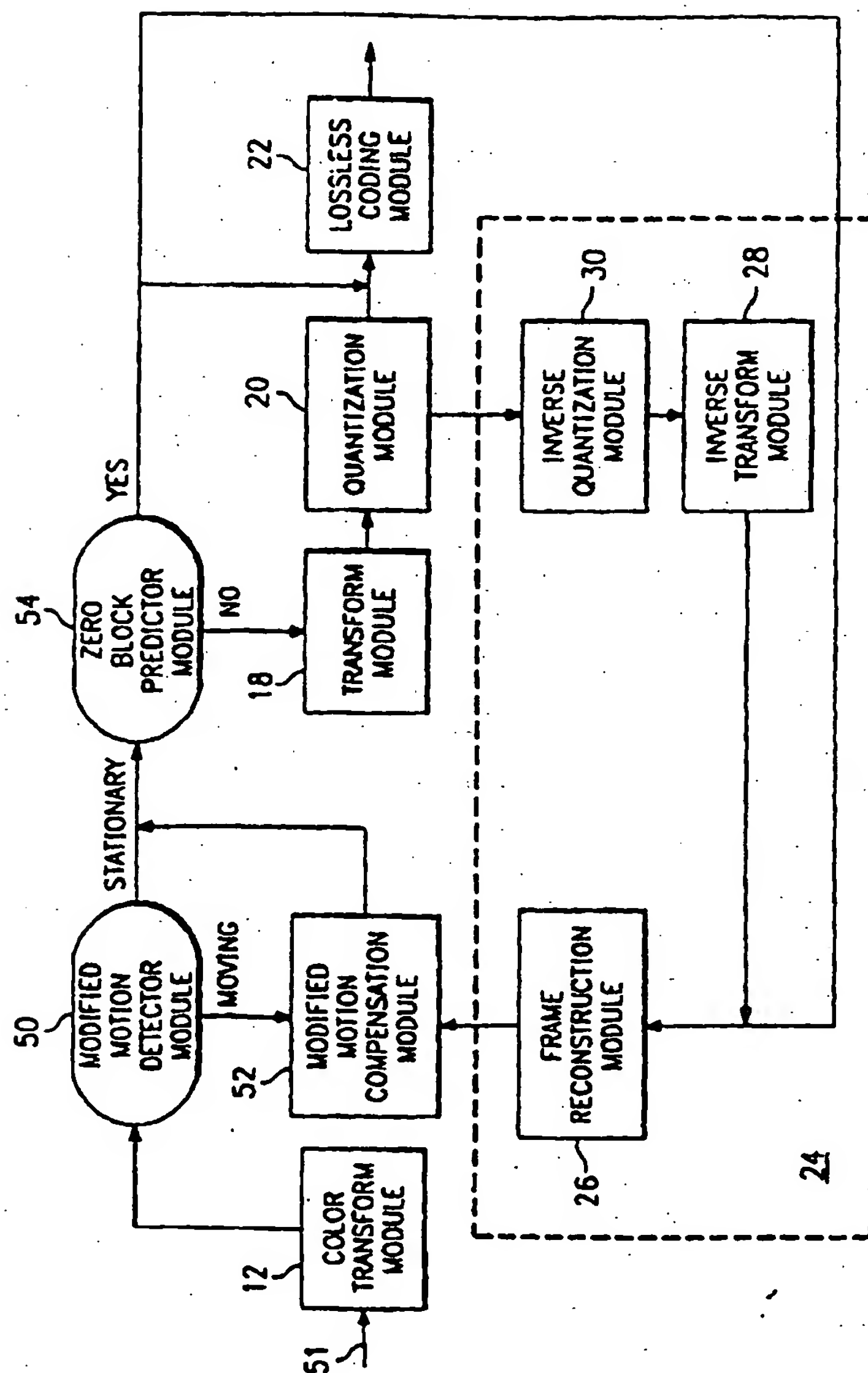


FIG. 3

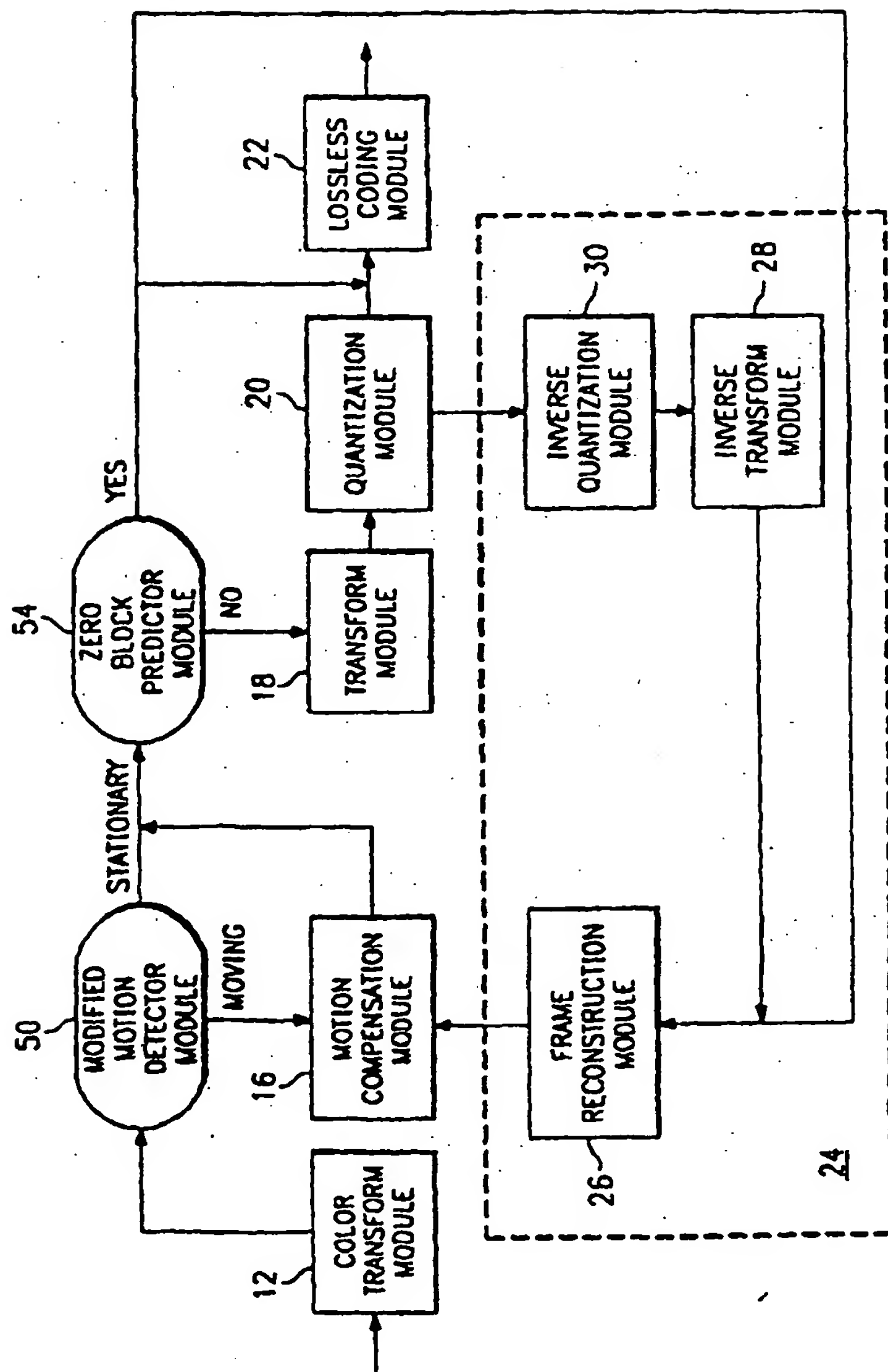


FIG. 5

FIG. 6

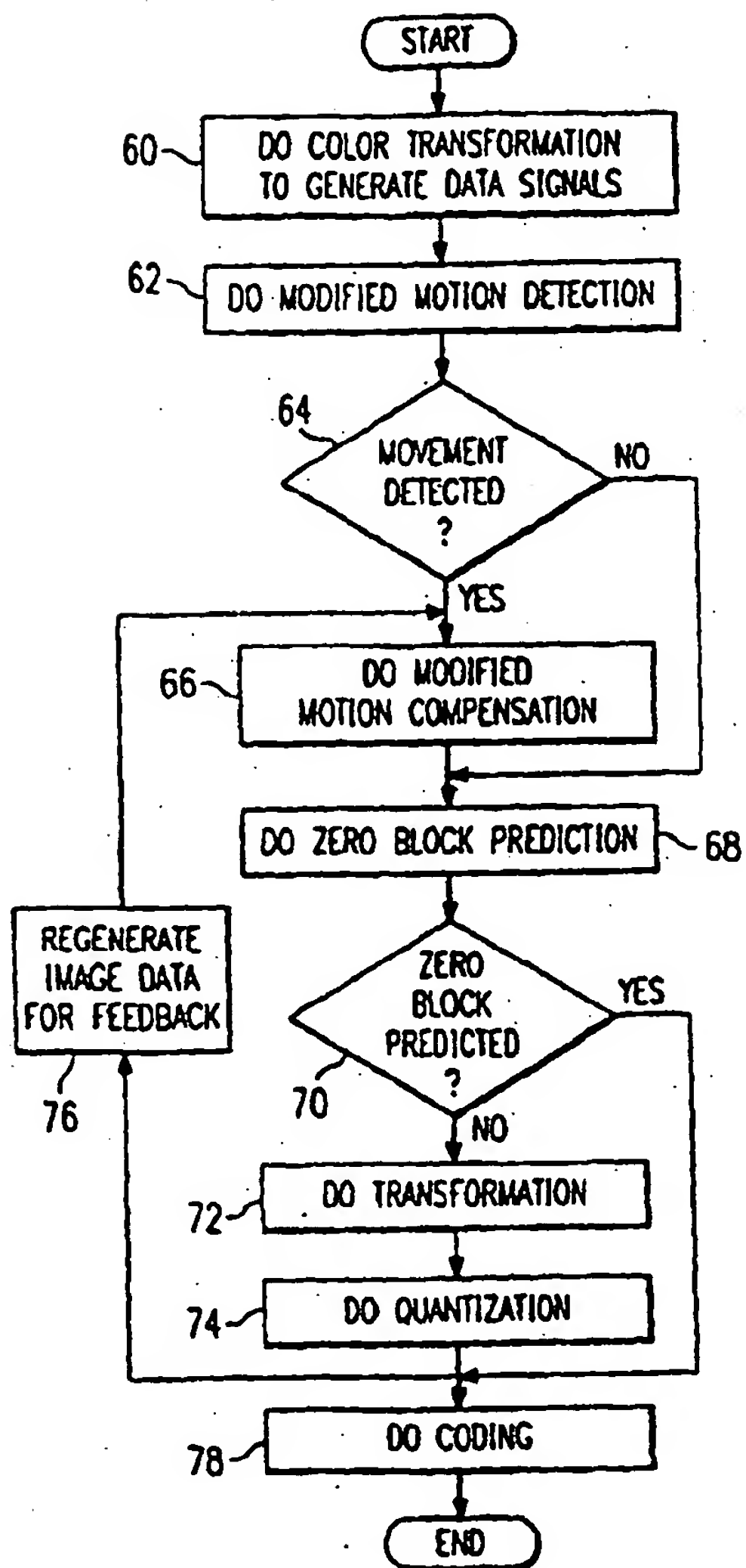


FIG. 9

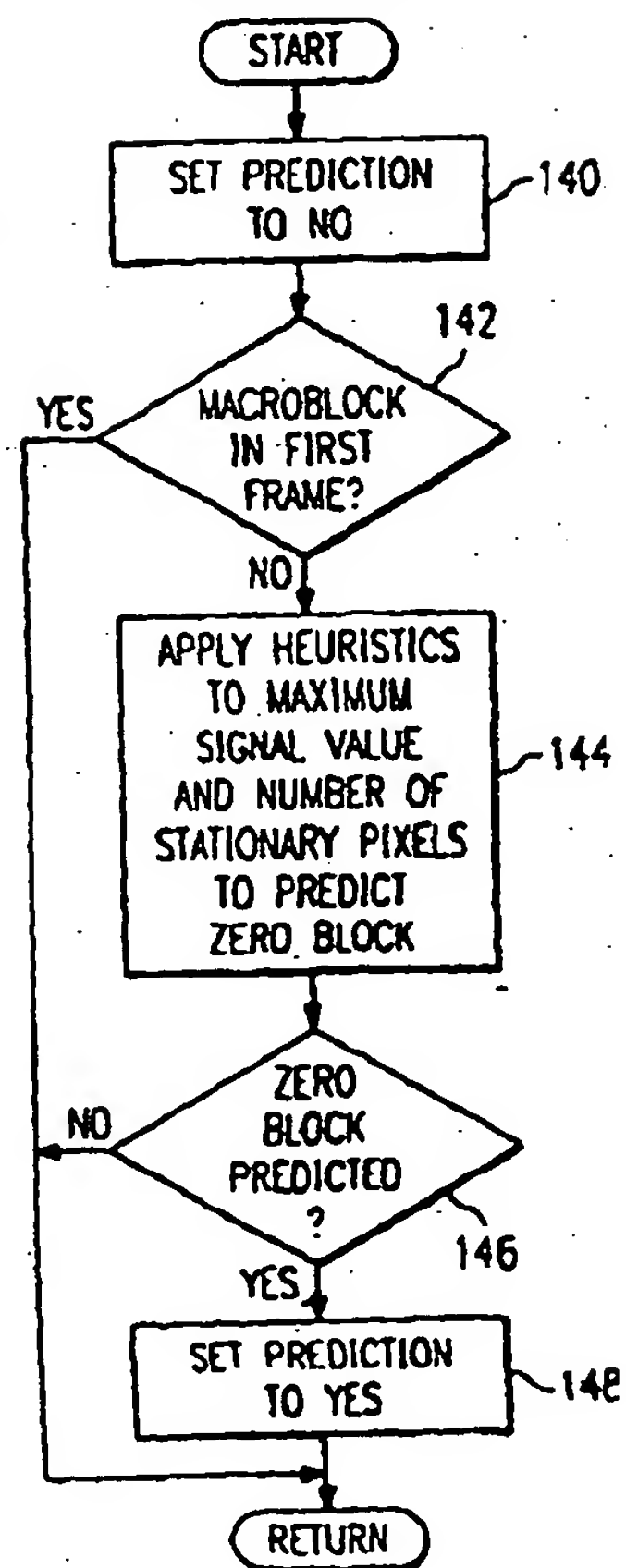


FIG. 7

